DDR SDRAM Signaling Design Notes

APRIL 1999
PRELIMINARY

OVERVIEW

Double Data Rate (DDR) SDRAM was defined by JEDEC 1997, and it was designed to be a natural migration from PC100 and PC133 SDRAMs to higher data rates. An evolutionary migration path was necessary to maintain the low cost legacy that SDRAMs provide for main memory platforms such as PC desktops, servers, and workstations. Low cost manufacturing was a predominant motivation for many of the device and system specifications. Many similarities exist between DDR SDRAMs and single data rate SDRAMs, including the 400mil TSOP-II packaging, command/ address protocols, and the DIMM and connector design. These similarities leverage off of the SDRAM manufacturing infrastructure and allow for the same test equipment, handlers, and manufacturing back-end equipment to be shared with SDRAM production. In fact, some manufacturers are even delivering SDRAM and DDR SDRAM made from the same die.

Some enhancements to the SDRAM definition were necessary to increase the device data rate to 266MHz. The new features include transmitting data on both positive and negative edges of the clock, reducing device input capacitance, adding on-chip delay locked loops (DLLs) to reduce access time uncertainty, adding data strobes to improve data capture reliability, and incorporating SSTL_2 signaling techniques.

The DDR device and system definitions yield many advantages to the device manufacturer, OEM, and end user. Typical PC266 DDR desktops will provide 2.0Gb/sec of memory bandwidth while also providing the lowest device access latency of high bandwidth DRAM technologies. Further, the V_{DD} and V_{DDQ} supply voltages have been reduced from 3.3V to 2.5V, so the power dissipation of PC266 devices will actually be lower than the power dissipation of PC100 and PC133 devices. Finally, PC266 devices will provide this improved performance at a device and system cost similar to SDRAMs. Virtually every DRAM supplier has already sampled DDR SDRAMs, which will be readily available in 1999. For more information on DDR SDRAMs, contact Micron Technology.

The PC266 motherboard design is very similar to current SDRAM motherboard designs, with the exception of the SSTL_2 signaling. The use of high-speed, low voltage signaling, such as SSTL_2, requires proper termination voltage and reference voltage design. Some attention must be paid to the generation and location of the termination voltage (V_{TT}) and reference voltage (V_{REF}) circuits, and to the placement and routing to the series and parallel termination resistors. This paper addresses these issues and provides a low-cost solution using the Micro Linear ML6554 voltage regulator.

TYPICAL APPLICATIONS

Figure 1 shows the block diagram of a typical PC266 main memory system, suitable for PC desktops and servers. There are variations to this diagram, based upon the number of modules supported by the system, whether non-buffered and registered modules are both supported by the system, and the designer's choice of clock topologies. In some applications, only one command/address bus is required. The controller chip is the PC north bridge, and it provides communication and control to the PCI adapter bus, the Accelerated Graphics Port (AGP) bus, the microprocessor host bus, and to the main memory.

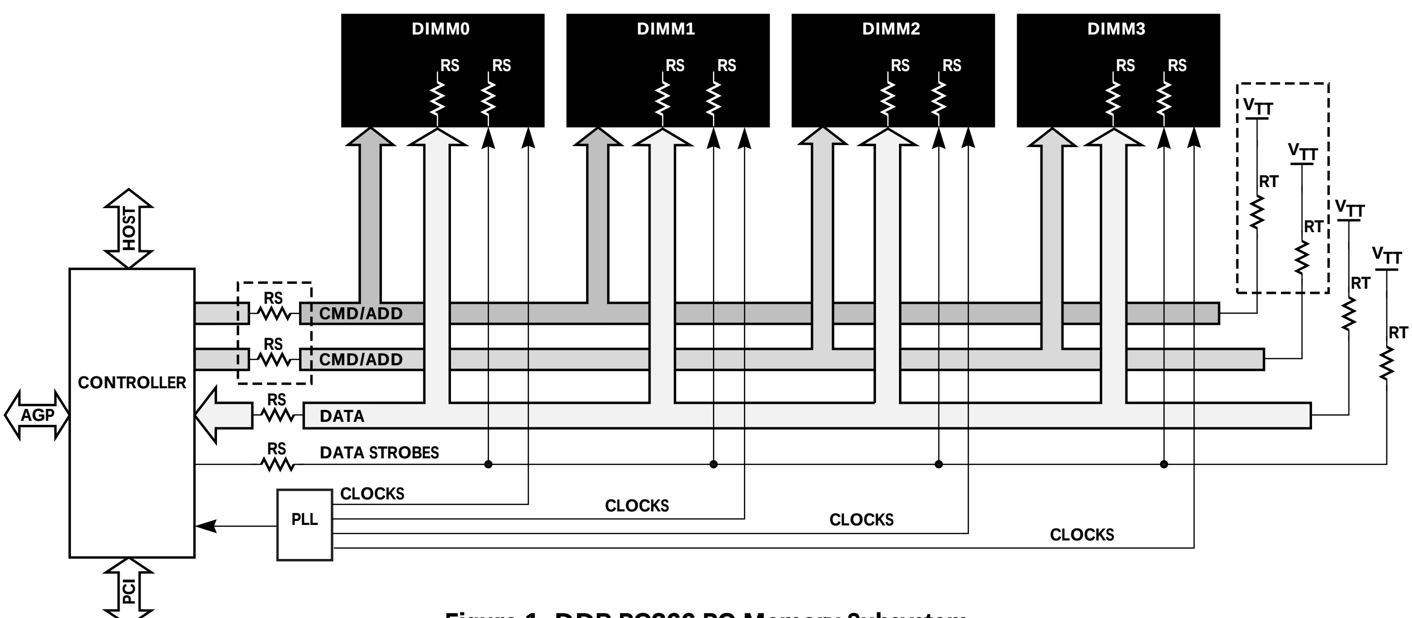

Figure 1. DDR PC266 PC Memory Subsystem

TYPICAL APPLICATIONS (Continued)

Command, address, and data signals are routed to the dual in-line memory modules (DIMM). The data signals include series resistors on the DIMMs and on the motherboard near the first DIMM socket, and they are parallel terminated to V_{TT} after the last socket. The data signals are double data rate and operate at 266Mbps, but the command/address signals only transition on positive clock edges at a 133Mbps single data rate. The DDR SDRAM input specifications allow the command and address signals to be received as either SSTL_2 or 2.5V LVCMOS signals. The use of termination resistors on the command/address signals is not necessary when LVCMOS drivers are used; however, the signal integrity and timing margins are improved by using SSTL_2 signaling.

SSTL_2

SSTL_2 stands for Series Stub Terminated Logic for 2.5V, and it was also defined and standardized within JEDEC. Although it is applicable for many different applications, SSTL_2 is particularly optimized for the main memory environment, which has long stubs off of the motherboard bus due to the DIMM routing traces. Figure 2 shows simplified driver and receiver topologies used in both LVTTL and SSTL_2. The output buffers for LVTTL and SSTL_2 are very similar and only differ in transistor size and supply voltage, V_{DDQ}. The reduced signal voltage levels of SSTL_2 allow the use of a 2.5V V_{DDQ}, which is compatible with the migration to lower DRAM supply voltages. It is possible to design a programmable output buffer that can be LVTTL or SSTL_2 compatible, as determined by the level applied to V_{DDQ}.

The LVTTL input receiver is typically an N-channel/P-channel stacked gate, as shown in Figure 2. The advantages of this topology are its simplicity and its very low power dissipation while receiving a steady state logic low or logic high signal. A fundamental disadvantage of the stacked receiver is that the threshold voltage matching of the top and bottom transistors are very poor over voltage, temperature, and process variation. The unpredictability of the switching threshold of this receiver, along with its relatively poor voltage gain, requires a larger input signal swing for reliable switching.

The SSTL_2 input receiver is typically a differential pair common source amplifier. This receiver provides better gain and bandwidth, and the variation in threshold voltage is much tighter, since the threshold voltage offset is determined by identical size and technology transistors in a differential pair configuration. The result is that smaller input signal swings can be used reliably. Many variations and enhancements to this input receiver topology are in use today.

Both LVTTL and SSTL input receivers can be turned off while the device is idle to minimize power dissipation, via disabling transistors not shown in the figure. However, the SSTL_2 input receiver will draw DC current while receiving steady state logic low or logic high inputs. To minimize system power dissipation, the DDR SDRAM receivers are turned off when not receiving active inputs, as controlled by the device protocol. With the exception of the CLOCK signal, all PC266 inputs are single-ended, and therefore, the second input to the receiver is the reference voltage, V_{REF}. It is important that V_{REF} stay symmetrically positioned between the logic high and logic low input levels over variations in process, voltage, and temperature so timing uncertainty will be minimized.

Figure 3 details the key parameters of the SSTL_2 specification. Note that the difference between V_{IH} and V_{IL} is now only 0.36V (2 x 0.18V), as compared to 1.2V with LVTTL. Also note that the minimum output voltage swing can be as small as 0.70V. V_{REF} is defined as 50% of V_{DDQ}, as V_{DDQ} can vary from 2.3V to 2.7V. In PC266 configurations, V_{REF} will be generated with 1% accuracy. The termination voltage, V_{TT}, is defined as being within 40mV of V_{REF}. The goal for the V_{REF} and V_{TT} circuits is to generate the V_{REF} and V_{TT} voltages that can track the midpoint of $V_{DDQ} – V_{SSQ}$ over environmental variations, and to be symmetric with respect to V_{OH} and V_{OL}. The V_{REF} and V_{TT} voltages must also track each other. These requirements can easily be met with a low-cost implementation using the ML6554 switching regulator.

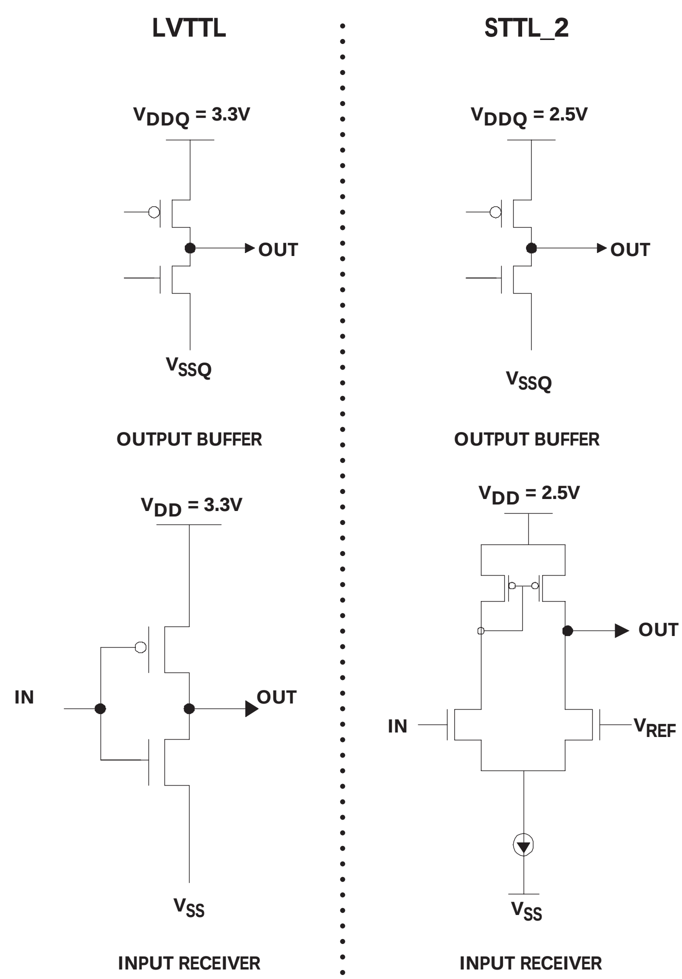

Figure 2. Comparison of LVTTL and SSTL_2 Drivers and Receivers

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DD}	Device Supply Voltage	V_{DDQ}		n/a	V
V_{DDQ}	Output Supply Voltage	2.3	2.5	2.7	V
V_{REF}	Input Reference Voltage	1.15	1.25	1.35	V
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V
INPUT DC LOGIC LEVELS					
V_{IH} (DC)	DC Input Logic High	V_{REF}+0.18		V_{DDQ}+0.3	V
V_{IL} (DC)	DC Input Logic Low	-0.3		V_{REF}-0.18	V
INPUT AC LOGIC LEVELS					
V_{IH} (AC)	AC Input Logic High	V_{REF}+0.35			V
V_{IL} (AC)	AC Input Logic Low			V_{REF}-0.35	V
OUTPUT DC CURRENT DRIVE					
I_{OH} (DC)	Output Minimum Source DC Current	-15.2			mA
I_{OL} (DC)	Output Minimum Sink DC Current	15.2			mA

Notes: V_{REF} and V_{TT} must track variations in V_{DDQ}.
Peak-to-peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC).
V_{TT} of transmitting device must track V_{REF} of receiving device.

Figure 3. SSTL_2 Key Specifications

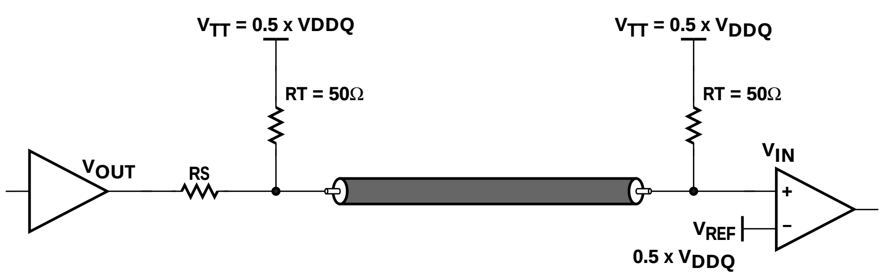

Figure 4a. SSTL_2 Double Terminated Output

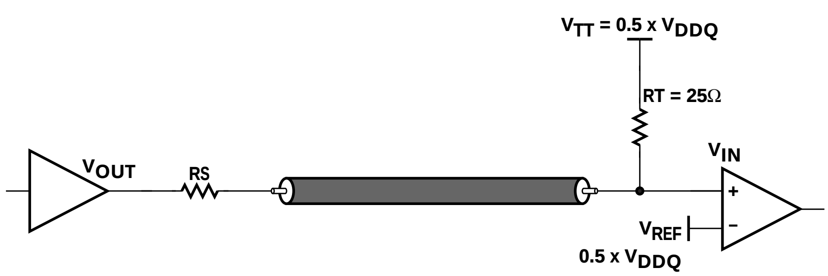

Figure 4b. SSTL_2 Single Terminated Output

The SSTL_2 specification requires adequate output current drive so that parallel termination schemes can be used. The use of parallel termination is important for high-speed signaling, since it allows proper termination of the bus transmission lines, which reduces signal reflections. The result will be improved settling, lower EMI emissions, and higher possible clock rates. A minimum termination resistance of 23Ω to V_{TT} can be used and still comply with the minimum output voltages and output currents of the SSTL_2 specification.

Two choices for implementing the parallel termination are shown in Figure 4. In Figure 4a, the bus is terminated at both ends with a 50Ω resistor, for a combined parallel resistance of 25Ω. In Figure 4b, the bus is terminated at the far end from the controller with a single 25Ω resistor. It is strongly recommended that the single resistor termination scheme in Figure 4b be used for best performance. The benefits of this approach include reduced cost, simpler signal routing, reduced reflections, and better signal bandwidth and settling.

The loaded characteristic impedance of this bus environment is on the order of 28Ω, when the effects of the distributed capacitance of the DIMM modules and components are considered for a fully populated system. So, the 25Ω resistor will provide a good match for the loaded impedance (considering board and device manufacturer tolerances), and the reflections will be terminated within a single round trip delay on the bus. In the dual termination approach, both ends of the bus are improperly terminated, and therefore, several round trip delays are required before the amplitude of reflections is diminished. The single termination scheme will reduce reflections on the bus, which will provide faster signal rise and fall times, and it will reduce the signal settling time, which will in turn reduce timing jitter due to intersymbol interference (ISI). Finally, the single termination resistor should be placed at the end of the bus farthest from the controller. This placement optimizes the signal integrity for signals transmitted from the controller to the DRAMs. This placement approach takes advantage of the fact that the signals transmitted in this direction must be reliably received by all DRAMs, while signals transmitted from the DRAMs only need to be received in one location – the controller. There are also more signals transmitted in this direction (command/address are unidirectional signals, while the data signals are bidirectional).

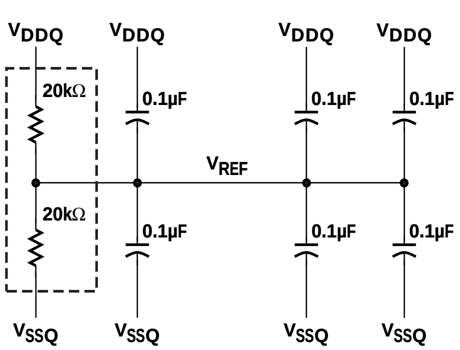

Figure 5. V_{REF} Network for PC266 DDR SDRAM

Series resistors are incorporated in the SSTL_2 signaling topology for main memory applications (referring back to Figure 1). 22Ω stub resistors are included on the data lines of the DDR DIMMs near the connector contacts to improve the signal integrity of the system. The stub resistors are very effective in dissipating the energy of the reflected waves travelling up and down the 30mm module traces, and they also help to isolate the stubs from the main memory bus. These resistors improve the signal settling times and transition times. A similar approach is used on PC100 DIMMs with 10Ω resistors on the data lines. The SSTL_2 stub resistors also provide a voltage divider with the parallel termination resistor to reduce the signal voltage swings on the bus. The reduced voltage swings provide headroom to V_{DDQ} and V_{SSQ} for signal overshoot, and therefore, maximum device input voltages are not threatened with this termination scheme.

The SSTL_2 series resistors also minimize on-chip I/O power dissipation, since some of the I/O power is moved off-chip and dissipated in the stub resistor. The nominal I/O power dissipation for this high-speed signaling scheme is about 19mW/pin, and only 7.5mW is dissipated on the device. In contrast, PC100 power dissipation is about 36mW/pin for a fully populated system operating at 100MHz due to the large signal swings and capacitive load. This low I/O power allows DDR SDRAMs to be used in PCs without requiring airflow or heatspreaders to cool the DRAMs.

REFERENCE VOLTAGE GENERATION

It is recommended that the input receiver reference voltage, V_{REF}, be generated with a simple resistor divider and globally distributed to the DIMMs, V_{TT} circuitry, and the controller. V_{REF} can be generated most accurately from a single circuit with global distribution, since offset and tracking errors of multiple circuits are eliminated. However, some attention should be paid to the routing of V_{REF}, since the SSTL_2 specification requires dynamic noise to be maintained to less than 2% of the V_{REF} DC level. The voltage offset from 50% of V_{DDQ} can easily be achieved with 0.5% or 1% accuracy using inexpensive discrete resistors. This topology provides excellent tracking to the 50% point over changes in voltage and temperature. Simple is better.

In order to maintain symmetry of V_{REF} with respect to V_{DDQ} and V_{SSQ} in the presence of switching noise, we recommend that V_{REF} be decoupled to both V_{DDQ} and V_{SSQ} with balanced decoupling capacitors. Decoupling to just one of these supplies can result in dynamic offsets from the 50% point if there is droop or collapse of the supply voltages during current transients. The V_{REF} signal becomes the input to a MOSFET gate in the input receiver, so it only has to supply small transient currents. We recommend that distributed decoupling capacitance be used to minimize the equivalent series inductance (ESL) and equivalent series resistance (ESR) of the decoupling network. The use of ceramic multilayer capacitors (MLCs) is also recommended for the same reasons.

Figure 5 shows the schematic diagram of a V_{REF} network suitable for PC desktop applications. We recommend using a decoupling capacitor at each DIMM socket location and a decoupling capacitor pair near the resistor divider. The capacitance network at the resistor divider will lower the equivalent AC output impedance of the divider. This decoupling will provide better termination of

REFERENCE VOLTAGE GENERATION (Continued)

noise voltages induced onto the V_{REF} line. The resistors shown in this figure may be eliminated when using the ML6554 switching regulator, since this device integrates the resistor divider on-chip. Either the ML6554 $VREF_{IN}$ or $VREF_{OUT}$ pins may be used to distribute the global V_{REF} instead; however, we recommend using $VREF_{OUT}$ to generate V_{REF} and achieve the lowest offset of V_{TT} relative to V_{REF}.

It is also necessary to keep V_{REF} as isolated from induced noise as possible. V_{REF} should be routed over a reference plane and isolated, and possibly shielded, from other noise sources. The V_{REF} signal is assigned to pin 1 on the 184-pin DDR DIMM, which is at one end of the connector. V_{SS} is also at the same end of the connector, so it is relatively easy to shield V_{REF} with V_{SSQ} on one side (V_{SS} and V_{SSQ} are usually shorted on the motherboard). If this shielding approach is used, V_{DDQ} should be routed on the opposite side of V_{REF} to maintain symmetry in the presence of noise on V_{DDQ} and V_{SSQ}. V_{DDQ} and V_{SSQ} should be "stitched" every 10-15mm to the associated reference plane to maintain a low impedance (inductance) connection to the plane. Figure 6 shows an example of the shielded V_{REF} PCB layout approach.

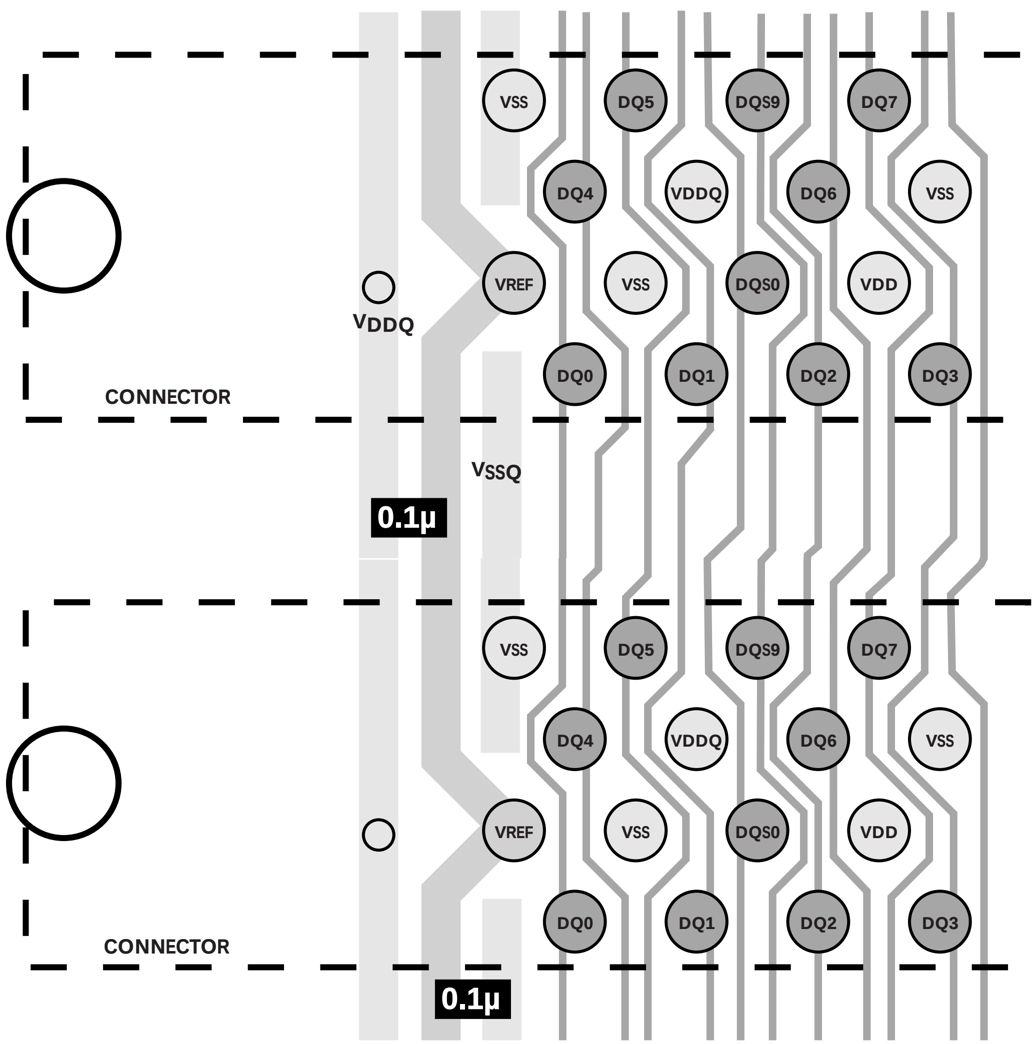

Figure 6. Shielded V_{REF} PCB Layout

TERMINATION VOLTAGE GENERATION

The V_{TT} generation circuit should be placed as close as possible to the parallel termination resistors to reduce the impedance and length of the signal return path. The parallel termination resistors should be placed just after the last DIMM socket to minimize the bus lengths. It's necessary to provide a low impedance connection from the termination resistors to V_{TT}. The V_{TT} side of the termination resistors should be placed on a wide V_{TT} island on the top signal layer, and decoupling capacitors should be distributed along the island to minimize the ESL and ESR of the decoupling network. A top signal layer V_{TT} island provides a good solution, since it eliminates additional vias that would be necessary to connect the signals to an internal V_{TT} plane (the termination resistors would be located on the top plane either way). Further, the island is located at the end of the bus, so it does not interfere with the signal routing. Figure 7 shows an example of the PCB layout for the V_{TT} island.

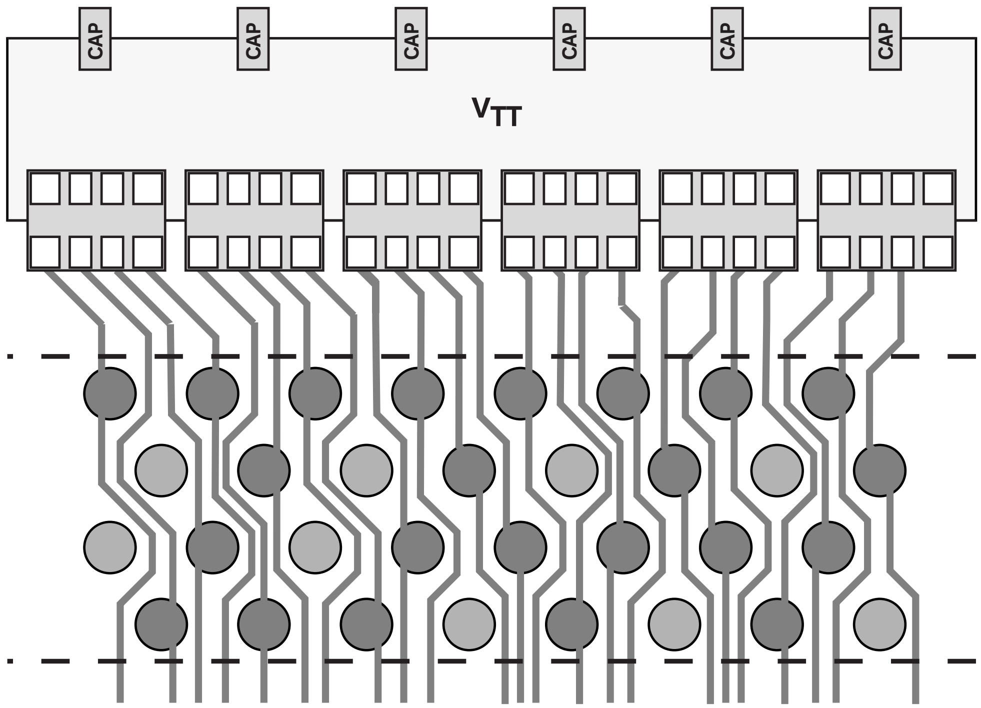

Figure 7. V_{TT} Island PCB Layout

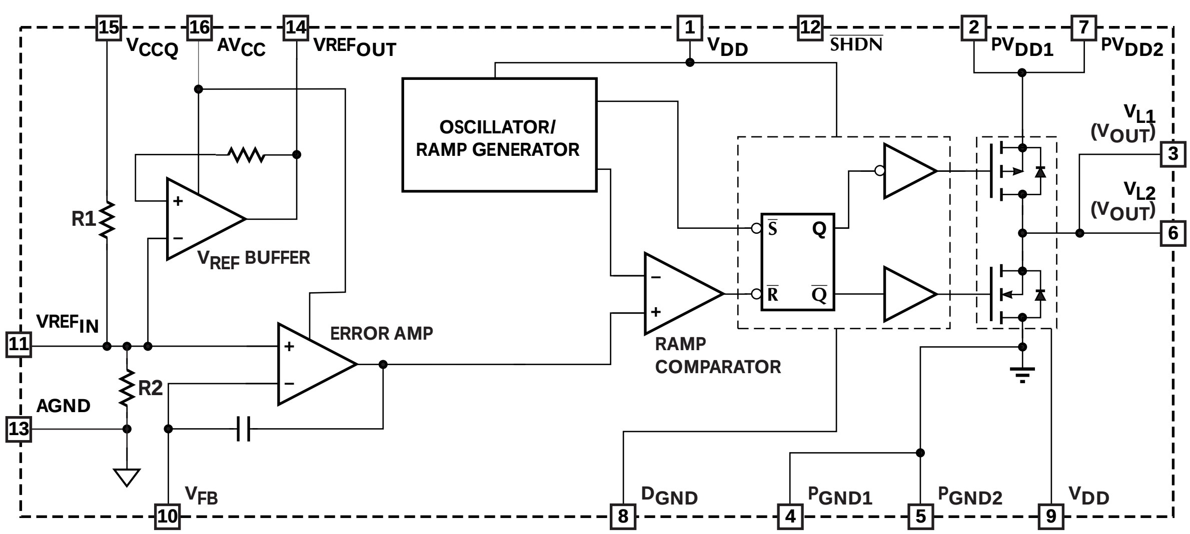

Figure 8. Micro Linear ML6554 Bus Terminator

TERMINATION VOLTAGE GENERATION (Continued)

The ML6554 switching regulator (Figure 8) is designed to convert voltage supplies ranging from 2.3V to 4V into a desired output voltage or termination voltage for various applications. The ML6554 can be implemented to produce regulated output voltages in two different modes. In the default mode, when the V_{REF} pin is open, the ML6554 output voltage is 50% of the voltage applied to V_{CCQ}. The ML6554 can also be used to produce various user-defined voltages by forcing a voltage on the $VREF_{IN}$ pin. In this case, the output voltage follows the input $VREF_{IN}$ voltage.

This switching regulator is capable of sinking and sourcing 3A of current without an external heatsink. The ML6554 uses a power surface mount package (PSOP) that includes an integrated heat slug. The heat can be piped through the bottom of the device and onto the PCB (Figure 10).

The ML6554 integrates two power MOSFETs that can be used to source and sink 3A of current while maintaining a tight voltage regulation. Using the external feedback, the output can be regulated well within 3% or less, depending on the external components chosen. Separate voltage supply inputs have been added to accommodate applications with various power supplies for the databus and power buses.

OUTPUTS

The output voltage pins (V_{L1}, V_{L2}) are tied to the databus, address, or clock lines via an external inductor capacitor filter. Output voltage is determined by the V_{CCQ} or $VREF_{IN}$ inputs.

INPUTS

The input voltage pins (V_{CCQ} or $VREF_{IN}$) determine the output voltages (V_{L1} or V_{L2}). In the default mode, where the $VREF_{IN}$ pin is floating, the output voltage is 50% of the V_{CCQ} input. V_{CCQ} can be the reference voltage for the databus.

Output voltage can also be selected by forcing a voltage at the $VREF_{IN}$ pin. In this case, the output voltage follows the voltage at the $VREF_{IN}$ input. Simple voltage dividers can be used in this case to produce a wide variety of output voltages between 2.3V to 4V.

V_{REF} INPUT AND OUTPUT

The $VREF_{IN}$ input can be used to force a voltage at the outputs. The $VREF_{OUT}$ pin is an output pin that is driven by a small output buffer to provide the V_{REF} signal to other devices in the system. The output buffer is capable of driving several output loads and can handle 3mA. The V_{REF} and V_{TT} accuracy (as implemented in Figure 8 at R1 and R2) is achieved internally using poly-resistors that are trimmed so that the V_{TT} (as shown in Figure 10) is 50% of the V_{CCQ}. Using careful internal layout and circuit design, offset between the V_{TT} and $VREF_{OUT}$ are guaranteed and tested to ±12.5mV.

FEEDBACK INPUT

The V_{FB} pin is an input that is used for closed loop compensation. This input is derived from the voltage output. See application section for recommendations (Figure 9).

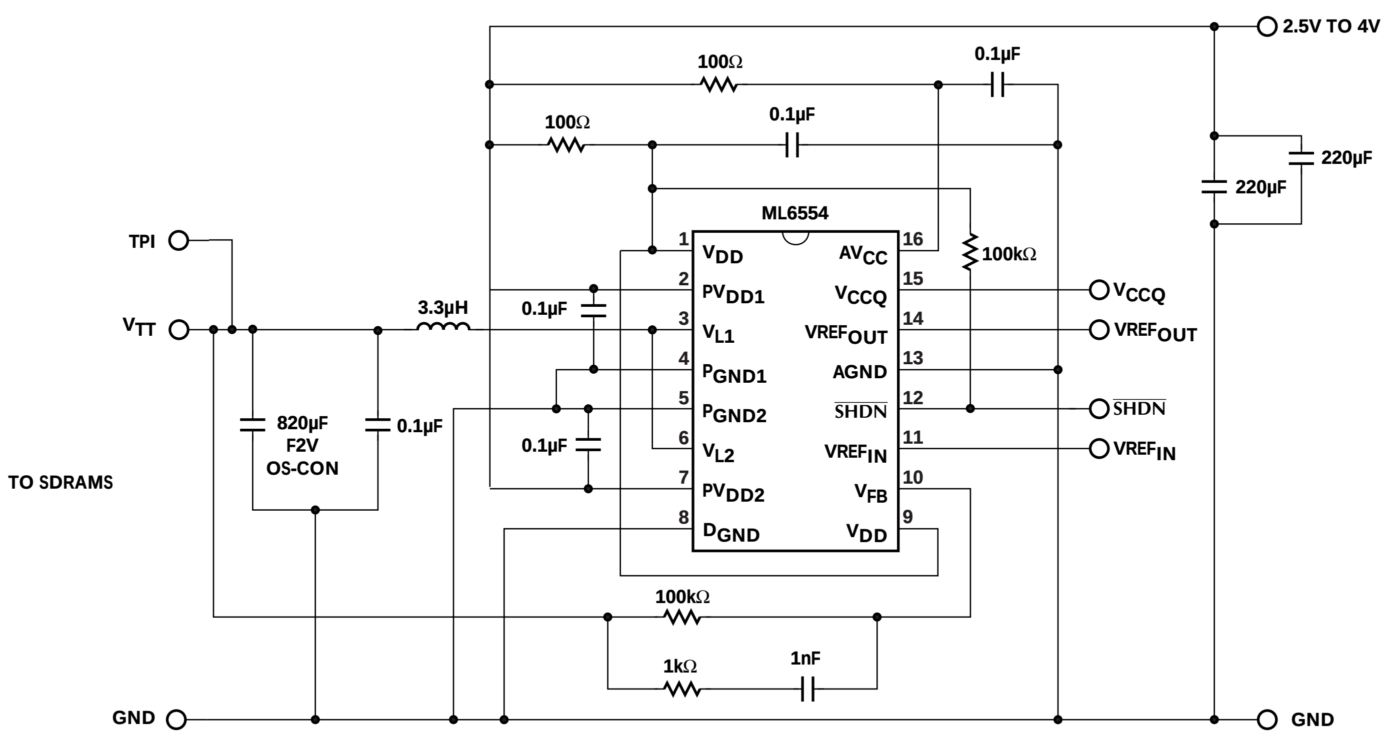

Figure 9. Micro Linear ML6554 Evaluation Board Schematic

TERMINATION VOLTAGE GENERATION (Continued)

USING THE ML6554 FOR SSTL BUS TERMINATION

The circuit schematic in Figure 9 shows a recommended approach for constructing a bus terminating solution for an SSTL_2 bus. The $VREF_{IN}$ pin should be left unconnected, while $VREF_{OUT}$ should be used to distribute V_{REF} using the decoupling network shown in Figure 5. The ML6554 can provide the voltage reference (V_{REF}) and terminating voltages (V_{TT}). Using the layout shown in Figures 11 through 13, the ML6554 delivered a V_{TT} ±20mV for 1A to 3A loads (Figure 14).

POWER HANDLING CAPABILITY OF THE PSOP PACKAGE

See Figure 10 for a cutaway view of the PSOP package. Also see the board layout shown in Figures 11 through 13. Make sure the heat slug is soldered to the board. At zero LFPM, the temperature around the package measured 55ºC for 3A loads. Note that a one ounce copper plane was used in the board construction.

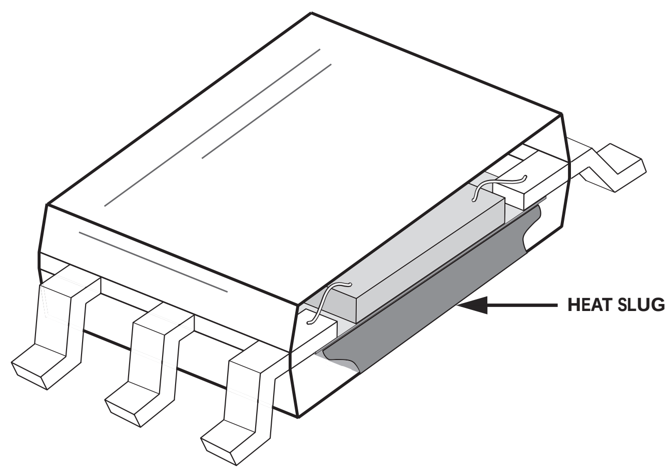

Figure 10. Cutaway view of PSOP Package

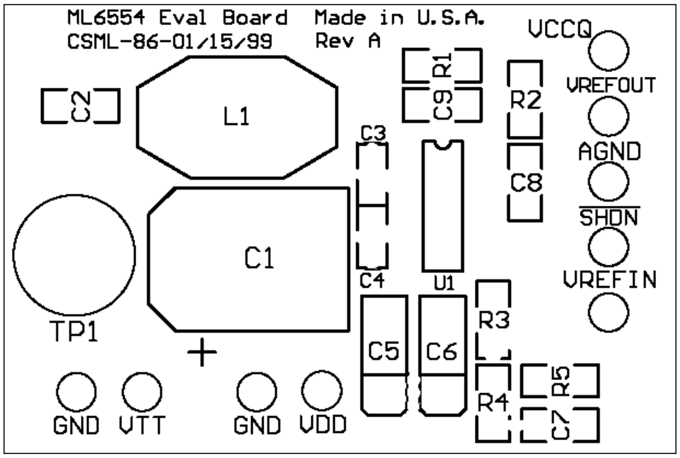

Figure 11. Top Silk

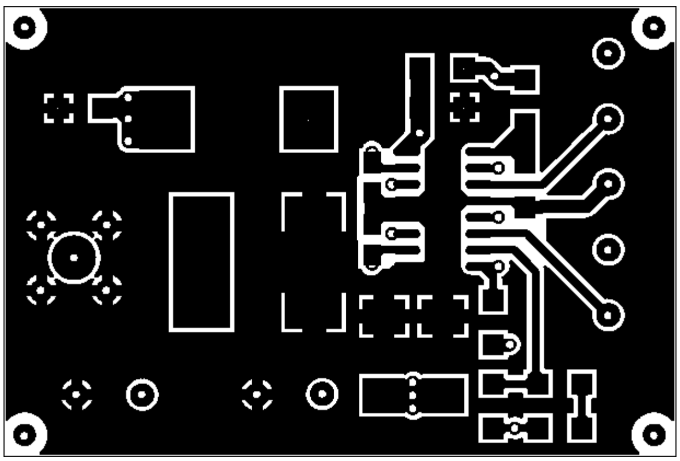

Figure 12. Top Layer

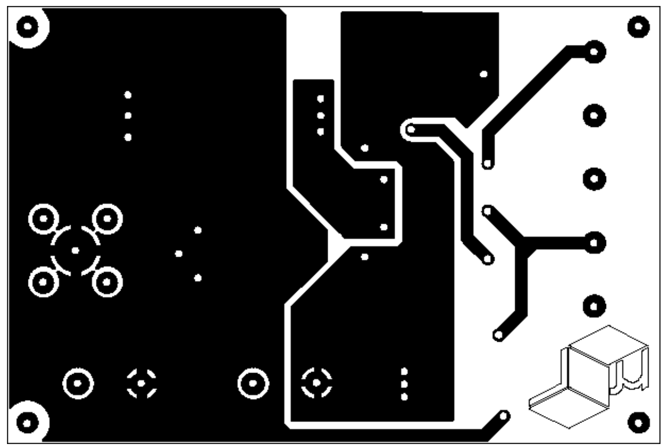

Figure 13. Bottom Layer

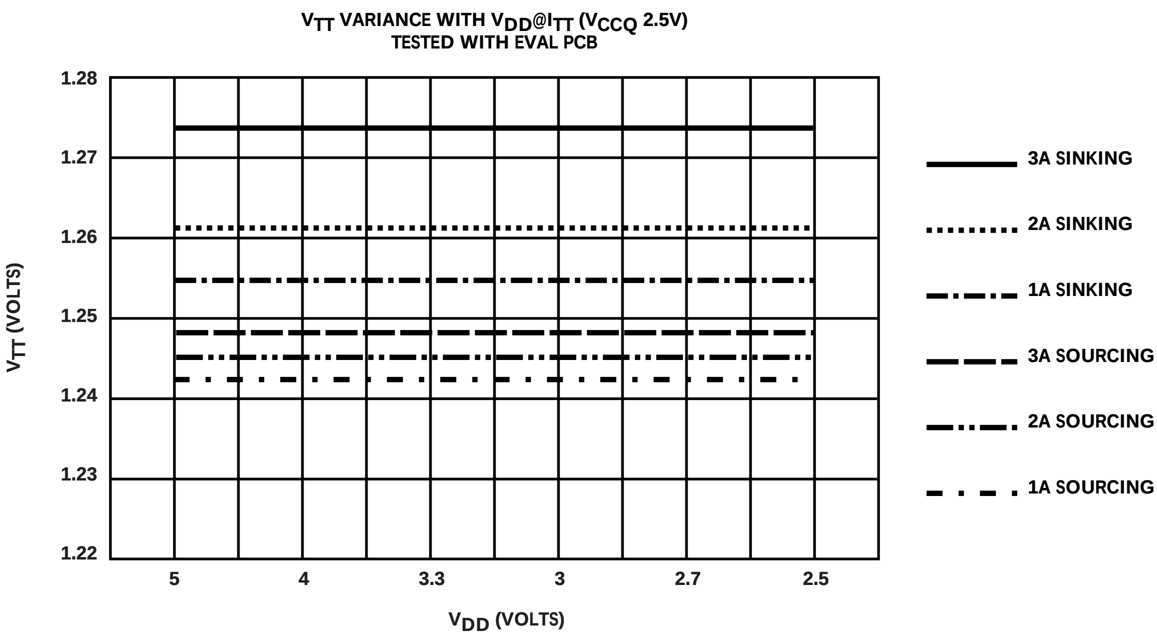

Figure 14. V_{TT} Performance for SSTL_2 Bus

TERMINATION VOLTAGE GENERATION (Continued)

DESIGN CONSIDERATIONS

Tailoring the ML6554 V_{TT} output with respect to the SSTL_2 specification (and a 3A output load current) will place constraints on the output components to fulfill the required task. This section will examine the transient capability of the output filter capacitor(s) to see how these components will affect overall performance. The specifications affected can be broken down into two distinct areas:

Equivalent Series Resistance (ESR)
Equivalent Series Inductance (ESL)

The ESR of the output bulk capacitors will primarily affect the capability to deliver a current surge within a specified delta voltage drop (ΔV) at V_{TT} out (Figure 15). With a given capacitor ESR, the ΔV drop will be proportional to the load current, and a step in output voltage will occur. (ΔVstep peak = ESR x I.) This step assumes a DC condition, i.e., no inductor ripple current. The SSTL_2 spec indicates a maximum delta voltage drop of 40mV. Assuming a 3A transient in one direction, the output capacitor ESR would allow a maximum INITIAL step of 40mV/ 3A, or 0.0133Ω (maximum ESR). Note that this does not give any margin for the slope condition when the output capacitor is sourcing (or sinking) current shown in Figure 15. Therefore, the capacitor ESR must be less than 13.3mΩ.

This step in voltage would be followed by a steady discharge of the output capacitor, resulting in a continued drop in the output voltage (Figure 16). During this discharge time, the V_{TT} output capacitor will continue to supply the current demand to the load until the ML6554 senses the drop in output voltage and provides an output "correction current" to compensate for the deviation in output voltage. Holdup time is a function of the output capacitor value and the time the ML6554 takes to respond to the drop in output voltage (due to the current slew rate of the inductor (ΔI / ΔT) and voltage feedback components). The feedback loop components will affect the holdup time required, since the feedback bandwidth is lower than the PWM switching frequency.

The ESL of the system will affect the output voltage in a transient manner. That is, a spike will appear on the V_{TT} output when a load current is demanded. The amplitude of the spike is related to the amount of current, the current switching speed, and the stray loop inductance in the circuit. $\Delta V = L \times (\Delta I / \Delta T)$ This is in addition to the aforementioned conditions. Thus, the primary issue in dealing with ESL on the V_{TT} plane is to reduce it as much as necessary. For example, the V_{TT} plane may have 20 multilayer film capacitors distributed over the plane area. The 1nH rating of a single cap will

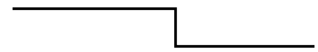

Figure 15. V_{OUT} Step

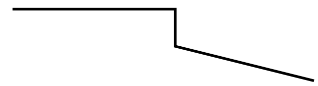

Figure 16. V_{OUT} Slope

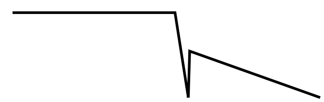

Figure 17.V_{OUT} Step+V_{SLOPE}+V_{SPIKE}

be effectively reduced to 50pH with 20 film caps in parallel. Using the equation above, this translates into a 75mV perturbation on the V_{TT} plane during a 3A transition in 2nS. With this information, higher current slew rates require lower stray inductance on the V_{TT} plane to keep voltage transients within the SSTL_2 spec. The combined effects are shown in Figure 17.

In order to obtain the best performance from the ML6554, all of these issues must be resolved to acceptable levels. It is interesting to note that SSTL requirements emphasize the need for low ESR/ESL components. Even a linear system requires a place to store the load current and the ability to keep the transient voltages below 40mV. For a given current, for either a linear or switching solution, the output ESR and ESL required are the same.

For a bus terminator, these issues become apparent when the full load current is taken all at once, at a fast slew rate (1-10nS). Another consideration is the potential of current slewing in both directions, first in one direction and then instantly in the other. The transient on the output capacitor would be 6A, requiring a further reduction in ESR and ESL to meet the SSTL_2 spec of 40mV. Knowing the required system performance will help in choosing the correct ESR and ESL values.

TERMINATION VOLTAGE GENERATION (Continued)

PCB LAYOUT

High-current, high-frequency PWM based DC/DC converters require the use of good layout practices. Current mirroring for PV_{DD} and GROUND traces will reduce stray lead inductance at the IC. Bypass capacitors should be placed as close to the IC as possible, especially at the PV_{DD} and GROUND pins. Good thermal management is also required. Ensure that sufficient copper area directly under the IC is available to aid in spreading the heat over a larger area on the PCB.

Directly under the ML6554 is a heat slug. This slug should make contact with the ground plane, which will act as a heat spreader. If copper under the IC is unavailable, a buried layer may be used as a heat spreader. Use vias to conduct the heat into the buried PCB layer. The vias should be small enough to retain solder when the board is wave-soldered.

For more information on the ML6554 Evaluation Board, please contact Micro Linear.

DISCLAIMER

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